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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/710,065 | 06/16/2004 | Brian T. Denton | BUR920040051US1 | 4064 |

23550 7590 02/12/2008

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|---|
| NORTON, JENNIFER L |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2121 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 02/12/2008 | ELECTRONIC |

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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/710,065
Filing Date: June 16, 2004
Appellant(s): DENTON ET AL.

Spencer K. Warnick
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 07 January 2008 appealing from the Office action mailed 02 July 2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

**WITHDRAWN REJECTIONS**

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. The rejection of claims 1-6 under 35 U.S.C. 101 has been withdrawn.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| **2004/0082083** | **Kraz et al.** | **10-2002** |
| **6,351,684** | **Shirley et al.** | **9-2000** |
| **6,535,783** | **Miller et al.** | **4-2001** |
| **6,711,450** | **Conboy et al.** | **2-2000** |
| **6,842,661** | **Chong et al.** | **9-2002** |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 12-18 are rejected under 35 U.S.C. 101.

2. Claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,842,661 (hereinafter Chong).

3. Claims 3 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of U.S Patent Publication No. 2004/0082083 (hereinafter Kraz).

4. Claims 11, 22 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view U.S. Patent No. 6,535,783 (hereinafter Miller).

5. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of U.S. Patent No. 6,711,450 (hereinafter Conboy).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Conboy in further view of U.S. Patent No. 6,351,684 (hereinafter Shirley).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Miller in further view of Conboy.

8. The following ground(s) of rejection are applicable to the appealed claims and were set forth in the Final Office Action mailed 02 July 2007, reproduced for completeness below:

Claims 12-18 are rejected under 35 U.S.C. 101. Claim 12, lines 1-2, the phrase "computer usable medium" has not been defined in the specification. Accordingly, when this phrase is given its broadest reasonable interpretation consistent with the specifications, "medium" is considered to include transitory waves and carrier waves. Such waves are not considered to be patentable subject matter, see O'Reilly v. Morse, 56 U.S. (15 How) 62 (1854).

Claims 1, 2, 4, 7-10, 12-16, 18-21, 23, 24, 26, 27 and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,842,661 (hereinafter Chong).

As per claim 1, Chong discloses a method comprising the steps of:

a. providing a floor schedule (Fig. 9, element 940) of an assembly unit (Fig. 9) for a device (col. 7, lines 29-35 and 59-67, col. 8, lines 26-32 and Fig. 9, element 910a and 910b); and

b. optimizing the floor schedule based on sensitivity data (col. 5, lines 10-26, col. 8, lines 48-52 and col. 9, lines 27-33) of the device (col. 10, lines 6-13) during operation of the assembly unit on the floor schedule (col. 5, lines 33-36 and col. 9, lines 27-41).

As per claim 2, Chong discloses the steps of receiving the sensitivity data and optimizing the floor schedule in real-time (col. 9, lines 27-41).

As per claim 4, Chong discloses the steps of generating sensitivity data for the device of an assembly unit during operation of the assembly unit on a floor schedule (col. 5, lines 10-14); and

receiving an optimal path data of the floor schedule based on the sensitivity data (col. 9, lines 4-8),

wherein the optimal path data controls the path of the device through the assembly unit (col. 10, lines 6-13 and 18-22).

As per claim 7, Chong discloses step b) further comprises a step of analyzing the sensitivity data of the device to estimate an amount of sensitivity of the device (col. 5, lines 10-23).

As per claim 8, Chong discloses step b) further comprises a step of analyzing the sensitivity data through at least one sensitivity model (i.e. predetermined electrical values for particular interconnect locations) to estimate an amount of sensitivity of the device (col. 5, lines 10-23).

As per claim 9, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

As per claim 10, Chong discloses a step of estimating a result of the at least one sensitivity model with a second sensitivity model (Fig. 9, element 950) in the case that data of the at least one sensitivity model is incomplete (col. 8, lines 39-52).

As per claim 12, Chong discloses a tangible computer program product (col. 8, lines 19-21 and col. 10, lines 36-42) comprising a computer useable medium (Fig. 9, element 932) having computer readable program code embodied therein for optimizing a floor schedule of an assembly unit for a device (col. 5, lines 33-36 and col. 9, lines 27-41), the program product comprising:

program code configured to analyze sensitivity data for the device during operation of the assembly unit on the floor schedule (col. 5, lines 33-36 and col. 9, lines 27-41); and

program code configured to optimize the floor schedule of the assembly unit based on the sensitivity data (col. 5, lines 10-26, col. 8, lines 48-52 and col. 9, lines 27-33).

As per claim 13, Chong discloses a program code configured to generate the sensitivity data for the device being assembled by the assembly unit (col. 5, lines 10-15 and col. 8, lines 48-52).

As per claim 14, Chong discloses the analyzing program code analyzes the sensitivity data through at least one sensitivity model (i.e. predetermined electrical values for particular interconnect locations) to estimate an amount of sensitivity of the device (col. 5, lines 10-23).

As per claim 15, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

As per claim 16, Chong discloses the analyzing program code further estimates a result of the at least one sensitivity model (Fig. 9, element 950) with a second sensitivity model in response to that data of the at least one sensitivity model is incomplete (col. 8, lines 39-52).

As per claim 18, Chong discloses the sensitivity data is received through a messaging system from at least one of the assembly unit and a testing unit (col. 5, lines 37-49 and col. 10, lines 36-42).

As per claim 19, Chong discloses an optimizer system comprising:

a model analyzer (Fig. 3, element 360) for receiving sensitivity data for a device of an assembly unit (col. 7, lines 25-29), and analyzing the sensitivity data during operation of the assembly unit on a floor schedule (col. 7, lines 29-35); and

a scheduling optimizer (Fig. 8, element 830) for optimizing the floor schedule of the assembly unit based on the analyzed sensitivity data (col. 7, lines 47-58 and col. 9, lines 27-33).

As per claim 20, Chong discloses a testing unit (Fig. 3, element 330) for generating sensitivity data for the device (col. 5, lines 10-14).

As per claim 21, Chong discloses the sensitivity data is received through a messaging system from at least one of the assembly unit and the testing unit (col. 5, lines 37-49 and col. 10, lines 36-42).

As per claim 23, Chong discloses wherein the sensitivity data is generated through at least one sensitivity model (col. 5, lines 17-25).

As per claim 24, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

As per claim 26, Chong discloses a method comprising the steps of:

generating sensitivity data (col. 5, lines 10-26 and col. 8, lines 48-52) for a device (col. 8, lines 32-40 and Fig. 9, element 910a and 910b) of an assembly unit during operation of the assembly unit on a floor schedule (col. 4, lines 60-63 and col. 5, lines 10-14); and

receiving an optimal path data of the floor schedule that is generated based on the sensitivity data (col. 9, lines 4-8),

wherein the optimal path data controls the path of the device through the assembly unit (col. 10, lines 6-13 and 18-22).

As per claim 27, Chong discloses the steps of generating the sensitivity data and receiving the optimal path data in real-time (col. 9, lines 27-41).

As per claim 29, Chong discloses the sensitivity data is transmitted through a messaging system (col. 5, lines 37-49 and col. 10, lines 36-42).

As per claim 30, Chong discloses the generating step further comprises the step of generating at least one sensitivity model with the sensitivity data (col. 5, lines 17-25 and 59-64).

As per claim 31, Chong discloses the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

Claims 3 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of U.S Patent Publication No. 2004/0082083 (hereinafter Kraz).

As per claim 3, Chong teaches to measuring electrical characteristics of devices formed across the semiconductors used to quantify the performance of the processing tools (col. 8, lines 48-52 and 55-58).

Chong does not expressly teach the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up data, hot electron data, mobile ion contamination data, and negative bias threshold instability data.

Kraz teaches to measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool (pg. 2, par. [0009], pg. 3, par. [0025], pg. 3-4, par. [0031]-[0032] and Fig. 2, element 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool to provide the automatic detection and response to an ESD event, in addition to providing advanced filtering of irrelevant ESD occurrences (including electrostatic discharge or electrostatic voltage) and the collection of valuable statistics on ESD environment for failure analysis and as evidence of compliance with customer's ESD requirements (pg. 3, par. [0028]).

As per claim 28, Chong teaches to measuring electrical characteristics of devices formed across the semiconductors used to quantify the performance of the processing tools (col. 8, lines 48-52 and 55-58).

Chong does not expressly teach the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up data, hot electron data, mobile ion contamination data, and negative bias threshold instability data.

Kraz teaches to measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool (pg. 2, par. [0009], pg. 3, par. [0025], pg. 3-4, par. [0031]-[0032] and Fig. 2, element 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool to provide the automatic detection and response to an ESD event, in addition to providing advanced filtering of irrelevant ESD occurrences (including electrostatic discharge or electrostatic voltage) and the collection of valuable statistics on ESD environment for failure analysis and as evidence of compliance with customer's ESD requirements (pg. 3, par. [0028]).

Claims 11, 22 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view U.S. Patent No. 6,535,783 (hereinafter Miller).

As per claim 11, Chong does not expressly teach wherein step b) further comprises a steps of inhibiting a failed tool of the assembly unit based on the sensitivity data; and optimizing the floor schedule to avoid the failed tool.

Miller teaches to inhibiting a failed tool of the assembly unit based on the data (col. 5, lines 58-62 and col. 6, lines 42-45); and optimizing the floor schedule to avoid the failed tool (col. 5, lines 62-67 and col. 6, lines 35-38).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include to inhibiting a failed tool of the assembly unit based on the data; and optimizing the floor schedule to avoid the failed tool to prevent the further production of faulty wafers by the tool (col. 7, lines 52-56).

As per claim 22, Chong teaches the testing unit further comprises a sensitivity monitor (Fig. 3, element 330) for generating sensitivity data (col. 5, lines 10-14);

a reliability generator (Fig. 3, element 310) for generating reliability data having rules for the device and assembly unit (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations); and

a tool controller (Fig. 3, element 350) for invoking the sensitivity monitor and reliability generator (col. 5, lines 17-23).

Chong does not expressly teach shutting down a testing tool of the testing unit.

Miller teaches shutting down a tool (col. 5, lines 58-62 and col. 6, lines 42-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include shutting down a testing tool of the testing unit to prevent the further production of faulty wafers by the tool (col. 7, lines 52-56).

As per claim 32, Chong teaches a testing unit comprising:

a sensitivity monitor (Fig. 3, element 330) for generating sensitivity data for a device (col. 5, lines 10-14);

a reliability generator (Fig. 3, element 310) for generating reliability data having rules for the device (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations); and

a tool controller (Fig. 3, element 350) for invoking the sensitivity monitor and reliability generator (col. 5, lines 17-23).

Chong does not expressly teach shutting down a testing tool of the testing unit (col. 5, lines 58-62 and col. 6, lines 42-45).

Miller teaches shutting down a tool (col. 5, lines 58-62 and col. 6, lines 42-45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include shutting down a testing tool of the testing unit to prevent the further production of faulty wafers by the tool (col. 7, lines 52-56).

As per claim 33, Chong teaches as set forth above a messaging system (col. 5, lines 37-49 and col. 10, lines 36-42) for transmitting the sensitivity data and reliability data in real-time (col. 9, lines 27-41).

As per claim 34, Chong teaches as set forth above at least one sensitivity model is generated with the sensitivity data (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

As per claim 35, Chong teaches as set forth above the sensitivity model includes a machine model (col. 5, lines 17-25 and 59-64; i.e. predetermined electrical values for particular interconnect locations).

Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of U.S. Patent No. 6,711,450 (hereinafter Conboy).

As per claim 5, Chong teaches step b) further comprises a step of testing of the device for sensitivities (col. 5, lines 10-14).

Chong does not expressly teach to prioritizing a testing of the device.

Conboy teaches to prioritizing the processing of a device (col. 6, lines 13-22).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include prioritizing the processing of a device to provide more flexibility in responding to changes in conditions (col. 5, lines 32-37).

As per claim 17, Chong teaches the optimizing program code tests the device for sensitivities (col. 5, lines 10-14).

Chong does not expressly teach to the optimizing program code prioritizes a testing of the device.

Conboy teaches to prioritizing the processing of a device (col. 6, lines 13-22).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong to include prioritizing the processing of a device to provide more flexibility in responding to changes in conditions (col. 5, lines 32-37).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Conboy in further view of U.S. Patent No. 6,351,684 (hereinafter Shirley).

As per claim 6, Chong in view of Conboy does not expressly teach the prioritizing step includes prioritizing the testing of a mask based on a size of a space on the mask.

Shirley teaches to testing a mask based on characteristics of a mask (col. 4, lines 54-67, col. 5, line 67 and col. 6, lines 1-17).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong in view of Conboy to include testing a mask based on characteristics of a mask to reduce wafer processing cycle time by knowing the exact location of the mask, providing flexibility of re-routing certain masks to the processing of more critical wafer lots due to business judgment rule, quality issue that has surfaced (col. 3, lines 24-29).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Miller in further view of Conboy.

As per claim 25, Chong in view of Miller as set forth above teaches the scheduling optimizer further comprises:

optimizing the floor schedule in real-time (col. 9, lines 27-41) based on the sensitivity data and the reliability data (col. 5, lines 10-26, col. 8, lines 48-52 and col. 9, lines 27-33).

Chong in view of Miller does not expressly teach automated material handling system dispatcher and a maintenance scheduler for scheduling maintenance based on the sensitivity data and the reliability data.

Conboy teaches to an automated material handling system dispatcher (col. 4, lines 3-11) and a maintenance scheduler for scheduling maintenance (col. 6, lines 62-67 and 8, lines 9-12).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Chong in view of Miller to include an automated material handling system dispatcher and a maintenance scheduler for scheduling maintenance to provide more flexibility in responding to changes in conditions (col. 5, lines 32-37).

**(10) Response to Argument**

Appellant's arguments (regarding Arguments; pgs. 4-9 of Appeal Brief), filed on 07 January 2008, have been fully considered but they are not persuasive.

Claims 1-2, 4, 7-10, 12-16, 18-21, 23-24, 26-27 and 29-31 are not anticipated under 35 U.S.C. 102(e) by Chong.

a. In response to Appellant's argument that "Chong does not disclose, *inter alia*, 'optimizing the floor schedule based on sensitivity data of the device'" with respect to claims 1, 12, 19 and 26 (see Brief, pg. 5, paragraph 1-2 and pg. 6, paragraph 1); the Examiner respectfully disagrees.

Appellant's definition (see Brief, pg. 5, paragraph 1) of "sensitivity" "refers to a degree of change in one thing in response to a unit amount of change in another thing. *(See,* e.g., *The American Heritage® Dictionary of the English Language, Fourth Edition,* sensitivity is "the degree of response of a receiver or instrument to an incoming signal or to a change in the incoming signal", recited in www.dictionary.com)."

Chong discloses "The system 300 also comprises a wafer electrical test (WET) unit 330 that is capable of performing a plurality of electrical tests that provide data relating to the electrical characteristics of various interconnect locations (e.g., contacts and/or vias) on the semiconductor wafers 105. The system 300 may comprise a

plurality of sub-controllers 350 that are capable of controlling various process steps that are performed on the semiconductor wafers 105. For example, the process controller 310 may provide predetermined electrical characteristic values, such as a predetermined resistivity value for particular interconnect locations, which may be used by the sub-controllers 350 to calculate control adjustments for various control process steps performed on the semiconductor wafers 105. A more detailed illustration and description of the sub-controllers 350 is provided in FIG. 4 and accompanying description below.

Additionally, the system 300 may comprise an interconnect control unit 360 that is capable of controlling the characteristics of interconnect locations, such as vias and contacts, on the semiconductor wafers 105. A more detailed illustration and description of the interconnect control unit 360 is provided in FIG. 8 and accompanying description below. **The system 300 is capable of performing various control adjustments to affect the characteristics of various interconnect locations on the semiconductor wafers 105, e.g., controlling the resistivity of a via and/or a contact.**" (Emphasis Added; col. 5, lines 10-36)

"Turning now to FIGS. 5-7, cross-sectional illustrations of a semiconductor wafer 105 with a trench and/or via is illustrated. FIG. 5 shows a ILD layer 520 that is deposited upon a substrate layer 530. Within the ILD layer 520, a trench 540 may be

formed. The trench 540 may be used to form various structures. In one embodiment, the trench 540 may be used to form a contact. In one embodiment, the trench 540 may be used to perform a damascene process, which may be used to create metal lines, contacts, and/or vias; however, other processes known to those skilled in the art having benefit of the present disclosure may be employed to create metal lines, contacts, and/or vias. The trench 540 may be lined with a barrier layer 510 to isolate the trench 540 from the ILD layer 520. Generally, the trench 540 may be filled with a metal such as tungsten or copper to form an interconnect location. Certain characteristics of the interconnect formed in the trench 540, e.g., resistivity, may influence the barrier liner control unit 410, which may adjust control parameters that affect the formation of the barrier layer 510. The barrier layer 510 is shown in more detail in FIG. 6. The barrier layer 510 may comprise a tantalum layer 610, a tantalum nitride layer 620, and an PMD layer 630. The tantalum nitride layer 620 may be positioned between the tantalum layer 610 and the PMD layer 630. Adjustments made to the PMD layer 630 may affect the barrier layer 510, which in turn may affect the characteristics of a contact formed from the trench 540. The ILD layer control unit 430 is capable of controlling the processing of the PMD layer 630, which may affect the barrier layer 510, thereby influencing the characteristic(s) of the trench 540. Adjusting the composition of the barrier layer 510 (e.g., a tantalum/tantalum-nitride/tantalum combination) may affect the characteristic (e.g., resitivity) of an interconnect. Additionally, adjusting the respective ratios of the film thickness of the

layers that form the barrier layer 510 (see FIG. 6) may affect the characteristic (e.g., resitivity) of an interconnect. Other metal deposition processes may be employed by embodiments of the present invention to affect the characteristic (e.g., resitivity) of an interconnect." (col. 5, lines 65-67 and col. 6, lines 1-35)

"Turning now to FIG. 8, a more detailed block diagram depiction of the interconnect control unit 360 is illustrated. The interconnect control unit 360 may receive metrology data relating to the processed semiconductor wafers 105. The metrology data may include measurements relating to the barrier layers 510, ILD layers 630, PMD layers 520, and/or trench formations used to form interconnect locations, etc. The interconnect control unit 360 may also receive control data from the sub-controllers 350, which may relate to control data that is influenced from the interconnect characteristics prescribed by the process controller 310. **Utilizing the metrology data and/or the control data, the interconnect control unit 360 may cause adjustments to be made upon a plurality of process steps performed on the semiconductor wafer 105 in order to affect the characteristics of the interconnect locations formed on the semiconductor wafers 105 (e.g., the resitivity of a contact or a via formed on the semiconductor wafer 105).**" (col. 7, lines 20-35)

"The **metrology data is directed to a variety of physical or electrical characteristics** of the devices formed across the semiconductor wafers 105. For example, metrology data may be obtained as to line width measurements, depth of trenches, sidewall angles, thickness, resistance, and the like." (col. 8, lines 50-55)

In summary, per Appellant's definition above, Chong discloses sensitivity data as to a change of electrical characteristics (e.g. resitivity) in response to a change metrology data (i.e. physical or electrical characteristics) and/or control data.

Further Chong, discloses "**Therefore, utilizing the sub-controllers 350, feedback and/or feed-forward control that affects electrical characteristics of the interconnect locations**, such as contacts and vias, may be achieved." (Emphasis Added; col. 7, lines 8-11)

"The Data relating to **feedback and/or feed-forward correction** may then be sent by the sub-controllers 350 to the computer system 930. The computer system 930 may then implement responsive control adjustment(s) to subsequent processes performed by the system 300." (col. 9, lines 4-8)

"Upon analysis of the metrology data and/or the WET data, the system 300 may implement an interconnect characteristic control process to affect the characteristics of

interconnect locations (e.g., vias, contact, etc.) on the semiconductor wafers 105 (block 1060). **Feedback and/or feed forward corrections** may be utilized to control interconnect characteristics formed on the semiconductor wafers 105." (col. 9, lines 27-33)

In summary, Chong discloses feedback correction to optimize the floor schedule (i.e. assembly units; per Appellants Specification, pgs. 4-5, paragraph [0008], "the floor schedule of an assembly unit (e.g. the tools, systems, methods, etc. that are used or available for use in a manufacturing environment to assemble a device, or a group of devices, such as an assembly lot") based on sensitivity data (i.e. electrical characteristics (e.g. resitivity)) of the device. Hence, Chong discloses Appellant's claimed limitation, "optimizing the floor schedule based on sensitivity data of the device".

b. With respect the Appellant's argument, "Chong does not enable an implementation of the claimed invention".

The Examiner does not question the enablement of issued patents. It is sufficient that Chong discloses the claimed invention as discussed above.

Claims 32-35 are not obvious under 35 U.S.C 103(a) Chong in view of Miller.

c. In response to the Appellant's argument that "Chong doe not discloses of suggest, *inter alia*, 'generating sensitivity data for a device [.]'" (see Brief pg. 7, paragraph 2); the Examiner respectfully disagrees.

The Examiner refers to the above response, pgs. 20-25, paragraph a. of this Examiner's Answer, and the argument herein as addressed.

Claims 3 and 28 are not obvious under 35 U.S.C 103(a) over Chong in view of Kraz.

d. In response to the Appellant's argument that "Chong also does not teach "the sensitivity data includes at least one of electrostatic discharge sensitivity data..."";

the Examiner respectfully disagrees.

The Examiner recognizes the Applicant has not accounted for the combination of Chong and Kraz under 35 U.S.C 103(a) for this limitation as set forth in the Final Office Action, mailed on 02 July 2007. Claims 3 and 28 recited below for convenience:

As per claim 3, Chong teaches to measuring electrical characteristics of devices formed across the semiconductors used to quantify the performance of the processing tools (col. 8, lines 48-52 and 55-58).

Chong does not expressly teach the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up

data, hot electron data, mobile ion contamination data, and negative bias threshold instability data.

Kraz teaches to measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool (pg. 2, par. [0009], pg. 3, par. [0025], pg. 3-4, par. [0031]-[0032] and Fig. 2, element 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to modify the teaching of Chong to include measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool to provide the automatic detection and response to an ESD event, in addition to providing advanced filtering of irrelevant ESD occurrences (including electrostatic discharge or electrostatic voltage) and the collection of valuable statistics on ESD environment for failure analysis and as evidence of compliance with customer's ESD requirements (pg. 3, par. [0028]).

As per claim 28, Chong teaches to measuring electrical characteristics of devices formed across the semiconductors used to quantify the performance of the processing tools (col. 8, lines 48-52 and 55-58).

Chong does not expressly teach the sensitivity data includes at least one of electrostatic discharge sensitivity data, electrical overstress sensitivity data, latch-up data, hot electron data, mobile ion contamination data, and negative bias threshold instability data.

Kraz teaches to measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool (pg. 2, par. [0009], pg. 3, par. [0025], pg. 3-4, par. [0031]-[0032] and Fig. 2, element 20).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to modify the teaching of Chong to include measuring and monitoring electrostatic discharge and electrostatic voltage for a process tool to provide the automatic detection and response to an ESD event, in addition to providing advanced filtering of irrelevant ESD occurrences (including electrostatic discharge or electrostatic voltage) and the collection of valuable statistics on ESD environment for failure analysis and as evidence of compliance with customer's ESD requirements (pg. 3, par. [0028]).

Kraz teaches "Thus, in accordance with the invention, an apparatus for monitoring an electrostatic discharge (ESD) occurrence in a semiconductor process tool that affects a device being processed by the semiconductor process tool is provided.

The apparatus comprises one or more sensors wherein each sensor is located adjacent to a part of the semiconductor process tool to detect an ESD occurrence near the part of the semiconductor process tool. The apparatus also has a control unit coupled to each sensor wherein the control unit has a processor that receives the signals from each sensor and generates ESD occurrence signals. The apparatus also has a semiconductor tool coupled to the control unit wherein the tool communicates a gating signal to the control unit corresponding to an event of the semiconductor tool which may expose a device to an ESD occurrence so that ESD occurrence signals that do not occur during the gating signal time period are filtered out." (pg. 2, paragraph [0009])

"In one embodiment, the process parameter event monitoring system may be used with any semiconductor process tool in which ESD occurrences may occur and it is desirable to determine the source, strength and frequency of those ESD occurrences (including electrostatic discharge or electrostatic voltage) in order to increase the yield of the semiconductor process. For example, with a die-attach tool, ESD occurrences (including electrostatic discharge or electrostatic voltage) may occur when the die picker contacts the die in a tape package prior to moving the die to bonding. The situation is aggravated by the fact that the die will become charged when it is separated from the tape. In addition, the combination of the rapid movement of the robotic arm of the die attach mechanism and insufficient ionization results in occasional discharges to the frame when the die is placed on the frame even through the bottom

of the die is an insulator. For the die attach tool, an ESD sensor may be placed on the moving arm next to the vacuum picker to provide instant information that an ESD discharge occurs when the die is touched or when the die is placed into a frame. Then, if an ESD occurrence has occurred, the die exposed to the ESD discharge may be isolated in a separate tray. The process parameter event monitoring system may be synchronized to the die attach tool using a vacuum relay signal (similar to the integrated circuit handler described in more detail below)." (pg. 3, paragraph [0025])

"FIG. 2 is an example of a process tool 20, such as a Integrated Circuit Handler, which incorporates a process parameter event monitoring system 22 in accordance with the invention. In this diagram, the various elements of the process tool 20 are not shown since those elements are well understood. Generally, the process parameter event monitoring system 22 comprises a control unit 24 (with computing resources) and one or more remote sensors 26 that are

placed near one or more points of interest in the process tool where process parameter events may occur. In the example shown in FIG. 2, the process parameter event monitoring system may detect ESD occurrences (ESD discharges or electrostatic voltages) that occur in the semiconductor process tool. In this example with the IC handler, the sensors are placed near a left robotic arm, near a first test socket, near a second test socket and near a right robotic arm. The invention is not limited to any particular number of sensors. The sensors are not described further herein as various

different sensors may be used with the invention. Examples of preferred ESD occurrence sensors that may be used with the invention are described in co-pending U.S. patent application Ser. No. 09/551,412 filed on Apr. 18, 2000 and entitled "Electrostatic Discharge and Transient Signals Monitoring System and Method" and co-pending U.S. patent application Ser. No. 09/876,200 filed on Jun. 6, 2001 and entitled "Apparatus and Method for Detection and Measurement of Environmental Parameters". ... Examples of other sensors for detecting other process parameters, such as pressure or temperature sensors, are well known and will not be described herein.

As shown in FIG. 2, the control unit 24 of the process parameter event monitoring system is connected to the tool's computer 28. For example, the control unit 24 may be connected to the tool's computer 28 by a well known RS232 interface or any other interface. The interconnection of the process parameter event monitoring system with the computer 28 of the tool permits the process parameter event monitoring system to communicate data with the process tool of the process tool's computer, permits the tool or the tool's computer to configure the process parameter event monitoring system and permits the automatic detection and handling of process parameter events (such as ESD occurrences (including electrostatic discharge or electrostatic voltage) in this example). Due to the construction of the sensors, no special cables are necessary to connect them to the control unit. For example, sensors placed on moving robotic arms utilize existing wiring already present in the wire harness of the arms as shown in FIG. 2. In particular, because ESD occurrences

generate electromagnetic signals in a very broad range, especially at high frequencies, a special coaxial signal is needed to pass the signal from the antenna to the monitor. In the case of this invention, the sensor incorporates antenna and processing means (i.e. A/D converter, microprocessor, etc. or simply a circuit that converts high-frequency signal into a lower-frequency data). The signal from that sensor is now capable of being communicated to the control unit via regular data wires without need of special coaxial cable because there is no RF signal present on these wires. The same cable between the control unit and the sensor supplies power to the sensor." (pgs. 3-4, paragraphs [0031]-[0032])

"In accordance with the invention, the gating method described above permits a process parameter event (such as an ESD occurrence) to be localized to a particular part of the process tool at a particular time. **There are also other methods in accordance with the invention for localizing a process parameter event (such as the ESD occurrence) and associating the events with a particular device being processed or a particular portion of the process tool.** One alternative technique is to place an additional sensor outside the tool or outside the process area. Then, if this external sensor picks up a process parameter event (such as a discharge) as well, or picks up an event at approximately the same or higher magnitude as the in-situ sensor, it can be safely assumed that this event originates elsewhere and not in the process tool. Another alternative technique for a process

parameter monitoring system that is detected ESD occurrences is to associate the detected ESD discharges with the presence or, specifically, change in static voltage at the point of measurements. The sensor described above in this case is capable of receiving static voltage as well as ESD discharges as is described in the co-pending patent application that was incorporated by reference above. A third alternate method is by triangulation of the source based on output of several sensors placed in the equipment. If several sensors pick up the same event, the output from these sensors can differ in magnitude based on distance from the event's origin. A simple well known calculation can determine which sensor was the closest one to the event thus improving localization. Any or all of the alternative techniques may be used independent of the gating method described above. In addition, any or all of the alternate techniques may be used in combination with the gating method described above. Now, the integrated operation of a semiconductor process tool with the process parameter event monitoring system will be described.

FIG. 10 is a flowchart illustrating the preferred integrated operation 50 of a semiconductor process tool with the process parameter event monitoring system. One of the biggest benefits gained from full integration of Event monitoring in the tool is **that the process of sorting out ICs that were exposed to dangerous levels of ESD can be automated and requires no operator assistance. When a test program is entered for each IC, ESD thresholds (damage and latent damage) are also entered as parameters. The software of the handler then sets**

**threshold of Event monitor for each point in accordance with IC damage level and antenna distance from the IC in process.** It is recommended that the level determined to cause latent damage be entered as the threshold. This way, all ESD occurrences (including electrostatic discharge or electrostatic voltage) below this level will be discarded by the Event monitor. As an example, the damage level of an IC is set to 200V CDM model and the latent damage threshold is set to 150V CDM. "Chip down" signals for each particular operation are communicated by the handler to Event monitoring system during operation of the handler. Event monitoring system provides IC handler with flow of data corresponding to magnitude of ESD occurrences (including electrostatic discharge or electrostatic voltage) at each particular location.

In step 52, the system determines that an ESD occurrence event has occurred. **In step 54, the system determines if the captured ESD occurrence is above the damage threshold. If an IC is exposed to ESD occurrence of stronger magnitude than the damage threshold, then IC handler would automatically place this IC into a separate tray in step 56. In step 58, the system determines if the ESD occurrence is above the latent threshold near the appropriate sensor near the IC in step 60.** If the IC experienced a lesser discharge, but still higher than the latent damage threshold, it can be automatically placed in a re-test tray in step 62 for future re-test and analysis by reliability engineer in step 64. Using this integrated process, the customer is assured that no IC that was exposed to excessive ESD levels is shipped to a customer. In addition, if too many

high-energy discharges occurred within short period of time, an alarm can sound, indicating problem in the tool and auto shutdown can be executed if desired. In addition, if the frequency of occurrence of weaker discharges is increasing on a tool, it may indicate that this tool may need preventive maintenance before discharges become damaging to the ICs." (pgs. 9-10, par. [0105]-[0107])

Furthermore, per Kirchhoff's Voltage Law, the sum of voltages around a loop is equal to zero, i.e. the electrostatic discharge voltage across the assembly unit is equal to the electrostatic discharge voltage across the device. Hence, Chong in view of Kraz teaches to Appellant's claimed limitation, "the sensitivity data includes at least one of electrostatic discharge sensitivity data..." of the device.

Whether claims 11 and 22 are not obvious under 35 U.S.C 103(a) over Chong in view of Miller.

e. In response to Appellant's argument, "Claims 11 and 22 are believed allowable based on their allowable base claims, respectively, as well as for their own additional features."; the Examiner respectfully disagrees.

The Examiner refers to the above response, pgs. 20-25, paragraph a. of this Examiner's Answer, and the argument herein as addressed.

Whether claims 5 and 17 are unpatentable under 35 U.S.C. 103(a) over Chong in view of Conboy (USPN 6,711,450).

f. In response to Appellant's argument, "Claims 5 and 17 are believed allowable based on their allowable base claims, respectively, as well as for their own additional features."; the Examiner respectfully disagrees.

The Examiner refers to the above response, pgs. 20-25, paragraph a. of this Examiner's Answer, and the argument herein as addressed.

Whether claim 6 is unpatentable under 35 U.S.C 103(a) over Chong in view of Conboy and further in view Shirley (USPN 6,351,684).

g. In response to Appellant's argument, "Claim 6 is believed allowable based on their allowable base claims, respectively, as well as for their own additional features."; the Examiner respectfully disagrees.

The Examiner refers to the above response, pgs. 20-25, paragraph a. of this Examiner's Answer, and the argument herein as addressed.

Whether claim 25 is unpatentable under 35 U.S.C 103(a) over Chong in view of Miller in further view of Conboy.

h. In response to Appellant's argument, "Claim 25 is believed allowable based on their allowable base claims, respectively, as well as for their own additional features."; the Examiner respectfully disagrees.

The Examiner refers to the above response, pgs. 20-25, paragraph a. of this Examiner's Answer, and the argument herein as addressed.

**(11) Evidence Appendix**

The Appellant has not submitted any evidence.

**(12) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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